REMARKS

Claims 3-10 and 21-27, 29, 30 and 32-35 are pending in the present application. Claims 21, 23 and 30 have been amended. Claims 28 and 31 have been canceled.

Claim Rejections-35 U.S.C. 103

Claims 3-10, 21 and 22 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Itonaga reference (U.S. Patent Application Publication No. 2002/0061639) in view of the Yu et al. reference (U.S. Patent Application Publication No. 2003/0029715). This rejection is respectfully traversed for the following reasons.

The method for fabricating a silicon on insulator semiconductor device of claim 21 includes in combination "subjecting the metallic silicide layer to a second heat treatment after said removing the protective layer, so that the metallic silicide layer has a low resistance crystalline structure, a sheet resistance of about 10 Ω/sq and a thickness of about 30 nm". Applicant respectfully submits that the method for fabricating a silicon on insulator semiconductor device of claim 21 would not have been obvious in view of the prior art as relied upon by the Examiner for the following reasons.

As described on page 15 of the present application, the metallic silicide layers of the silicon on insulator (SOI) device as shown in Fig. 10 have low regular sheet resistance of about 10 Ω/sq and are very thin (30 nm). Applicant respectfully emphasizes that only the Itonaga reference as relied upon makes mention of SOI technology, but however apparently only in a very general manner as in paragraph

[0141]. Accordingly, the prior art taken as a whole thus does not disclose a method of manufacturing a silicon on insulator device including subjecting a metallic silicide layer to a second heat treatment so that the metallic silicide layer has a low resistance crystalline structure, a sheet resistance of about 10 Ω/sq and a thickness of about 30 nm. This should be evident because the Yu et al. reference is generally directed to a method and apppartus for annealing materials deposited in a process chamber, and the Yu et al. reference is generally directed to fabrication of a MOSFET.

It is thus unclear how the secondary prior art would provide the necessary motivation to modify the teaching of the Itonaga reference, which is principally directed to a MISFET on a semiconductor substrate, to provide a method of fabricating an SOI device including a second heat treatment so that a metallic silicide layer has a low resistance crystalline structure, a sheet resistance of about 10 Ω/sq and a thickness of about 30 nm, as would be necessary to meet the features of claim 21. Applicant therefore respectfully submits that the method for fabricating a silicon on insulator semiconductor device of claim 21 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 3-10, 21 and 22, is improper for at least these reasons.

Claims 23-29 have been have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Itonaga reference in view of the Yu et al. reference, in further view of the Wu reference (U.S. Patent No. 6,534,405). This rejection is respectfully traversed for the following reasons.

The method of manufacturing a silicon on insulator semiconductor device of claim 23 includes in combination "forming a metallic layer having an orientation of a (200) surface on the silicon layer on the heated substrate by a straight sputtering method"; and "subjecting the first metallic silicide layer to a second heat treatment after said removing the protective layer, so as to change the first metallic silicide layer into a second metallic silicide layer having a low resistance crystalline structure and a thickness of about 30 nm". Applicant respectfully submits that the prior art as relied upon by the Examiner does not make obvious these features.

The Yu et al. reference in paragraph [0069] teaches a deposition process whereby the substrate is maintained at a temperature between about 10° C and about 500°C, preferably about 50°C and about 300°C, and most preferably between about 50° C and about 100°C. Accordingly, the preferred substrate temperature range as taught by the Yu et al. reference is a range between about 50° C and about 100°C. This reference does not specifically teach forming a metallic layer of an SOI device wherein deposition temperature of a metallic layer is in a specific range of between 200° C and 400°C, so that the metallic layer surface may have a strong orientation of (200). Since surface orientation is not an issue or factor under consideration in the prior art, it is unclear how motivation may be drawn from the relied upon prior art to modify the teaching of the Itonaga reference for example, to provide a method of manufacturing an SOI device that uses a metallic layer deposition temperature within a specific range of 200° C and 400°C to provide the metallic layer as having an orientation

of a (200) surface. That is, although a very broad deposition range is initially disclosed in the Yu et al. reference, the specific range as featured in claim 23 is not suggested. Applicant therefore respectfully submits that the method of manufacturing a silicon on insulator semiconductor device of claim 23 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 3-27 and 29 is improper for at least these reasons.

Claims 30-35 have been have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Itonaga reference in view of the Yu et al. reference, in further view of the Liaw reference (U.S. Patent No. 6,413,803). This rejection is respectfully traversed for the following reasons.

The method of manufacturing a silicon on insulator semiconductor device of claim 30 includes in combination "heating the substrate to a temperature equal to or higher than about 200°C and lower than about 400°C". Applicant respectfully submits that the prior art as relied upon by the Examiner does not make obvious these features.

The Examiner has relied upon paragraph [0068] of the Yu et al. reference as teaching a predetermined temperature range of between 10°C - 500°C. However, the Yu et al. reference does not teach a specific temperature deposition range of equal to or higher than about 200°C and lower than about 400°C as featured in claim 30, that would result in a stronger orientation of a (200) surface as described on page 12 of the present application. Applicant therefore respectfully submits that the method of manufacturing a silicon on insulator semiconductor device of claim 30 would not have

been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 30 and 32-35 is improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

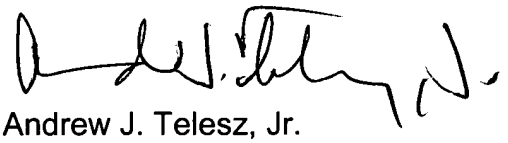
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to September 17, 2006, for the period in which to file a response to the outstanding Office Action. The required fee of $120.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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